This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS

1. (cancelled)

E1

2. (currently amended) A method of making a multi-layer circuit assembly comprising the steps of:

(a) providing a core structure including an inner dielectric element having first and second metal layers on opposite surfaces thereof;

(b) forming one or more through vias extending through said metal layers and said inner dielectric element;

(c) coating said metal layers and said through vias with a dielectric material to thereby form a coated structure having first and second outer dielectric layers overlying the first and second metal layers respectively and dielectric material lining said through vias;

(d) providing outer metal layers over said first and second outer dielectric layers;

(e) metallizing said coated through vias to form metallic via liners connecting said outer metal layers and insulated from said first and second metal layers; and

(f) patterning said outer metal layers such that at least some of said metallic via liners are electrically isolated from said first and second metal layers, ~~The method as claimed in claim 1~~ wherein said patterning of said outer metal layers forms first signal lines overlying and substantially parallel to the plane of said first metal layer and second signal lines overlying and substantially parallel to the plane of said second metal layer.

3. (withdrawn) A method as claimed in claim 2~~1~~, wherein said first metal layer includes a ground plane and said second metal layer includes a power plane.

4. (previously presented) The method as claimed in claim 2, wherein said first signal lines are substantially perpendicular to said second signal lines.

5. (currently amended) The method as claimed in claim ~~1~~-2 further comprising the steps of forming blind vias through said outer dielectric layers to expose one or more regions of said first and second metal layers and metallizing said blind vias so that at least some of said first and second signal lines are connected to said first and second metal layers.

E1

6. (previously presented) The method as claimed in claim 5 wherein said steps of metallizing said blind vias and metallizing said through vias are performed simultaneously.

7. (previously presented) The method as claimed in claim 2, further comprising the step of forming additional signal lines in at least one of said first and second metal layers before the coating step.

8. (currently amended) The method as claimed in claim ~~1~~-2, wherein each said through via has side walls, said side walls being covered by said dielectric material during the coating step.

9. (currently amended) The method as claimed in claim 2, wherein said ~~the selectively~~ patterning ~~step~~ includes ~~the step of~~ selectively removing portions of said ~~the~~ outer metal layers.

10. (currently amended) The method as claimed in claim 9 wherein said portions of said outer metal layers are selectively removed by ~~the selectively patterning step includes the step of selectively~~ etching ~~the outer metal layers to form said first and second signal lines therein~~.

11. (currently amended) The method as claimed in claim 5, wherein the step of providing outer metal layers over said ~~the~~ first and second outer dielectric layers includes the step of:

depositing a seed layer over said outer dielectric layers including the blind vias and the exposed regions of said first and second metal layers;

plating or sputtering a metal onto said seed layer.

E1

12. (currently amended) The method as claimed in claim 2 wherein said ~~step of selectively patterning said~~ outer metal layers ~~includes the step of~~ are patterned by a step including selectively depositing said outer metal layers over said outer dielectric layers.

13. (previously presented) The method as claimed in claim 5, wherein the step of forming said blind vias includes the step of laser drilling said outer dielectric layers.

14. (currently amended) The method as claimed in claim 13, further comprising the step of plasma etching said blind vias after the laser drilling step to remove ~~any said~~ dielectric material residue remaining in said blind vias.

15. (currently amended) The method as claimed in claim 2~~1~~, wherein during the coating step said dielectric material is provided having a uniform thickness.

16. (currently amended) The method as claimed in claim 2~~1~~, wherein after the coating step said dielectric material has a uniform thickness of approximately 25-75 microns.

17. (currently amended) The method as claimed in claim 2~~1~~, wherein after the coating step said through vias remain open.

18. (currently amended) The method as claimed in claim 2~~1~~, wherein said through vias have a diameter of approximately 175-200 microns before the coating step and approximately 25-150 microns after the coating step.

19. (currently amended) The method as claimed in claim 2~~1~~, wherein the coating step includes the step of electrophoretically depositing said dielectric material.

20. (withdrawn) A method as claimed in claim 2~~1~~, wherein the coating step includes the step of dipping said core structure in said dielectric material.

21. (withdrawn) A method as claimed in claim 2~~1~~, wherein the coating step includes the step of spin coating said core structure with said dielectric material.

22. (currently amended) The method as claimed in claim 2~~1~~, wherein the step of forming said through vias includes the steps of etching said first and second metal layers and drilling said inner dielectric element.

23. (withdrawn) A method as claimed in claim 2~~1~~, wherein the step of forming said through vias includes punching said first and second metal layers and said inner dielectric element.

24. (withdrawn) A method as claimed in claim 21, wherein the step of forming said through vias includes the step of plasma etching.

25. (currently amended) The method as claimed in claim 21, wherein the step of forming said through vias includes the steps of:

etching said first and second metal layers to provide aligned openings therein;

aligning a laser in one of said aligned openings and drilling said inner dielectric element.

26. (currently amended) The method as claimed in claim 21, wherein said first and second metal layers are approximately 1-18 microns thick.

27. (currently amended) The method as claimed in claim 21, wherein said inner dielectric element is approximately 25-50 microns thick.

28. (cancelled)

29. (currently amended) A method of making a multi-layer circuit assembly comprising the steps of:

(a) providing an inner dielectric element;

(b) providing first and second metal layers having openings therein on opposite surfaces of said inner dielectric element, said openings defining edges in said first and second metal layers, each said opening in said first metal layer being in substantial alignment with one of said openings in said second metal layer;

(c) coating said inner dielectric element and said first and second metal layers and said edges of said first and second metal layers with a dielectric material to thereby form a coated structure having first and second outer dielectric layers covering said first and second metal layers respectively and having dielectric material in said openings of said first and second metal layers and covering said edges of said first and second metal layers;

(d) forming one or more through vias extending through said coated structure, each said through via being in substantial alignment with said aligned openings in said first and second metal layers;

(e) providing first and second outer metal layers covering said outer dielectric layers;

(f) metallizing said through vias to form metallic via liners connecting said outer metal layers, and insulated from said first and second metal layers, said dielectric material extending into said vias being disposed between the metallic via liners and said first and second metal layers; and

(g) patterning said outer metal layers such that at least some of said metallic via liners are electrically isolated from said first and second metal layers, ~~The method as claimed in claim 28~~ wherein said patterning of said outer metal layers forms first signal lines overlying said first metal layer and second signal lines overlying said second metal layer.

30. (currently amended) The method as claimed in claim 29~~28~~ further comprising the steps of forming blind vias through said outer dielectric layers to expose one or more regions of said first and second metal layers and metallizing said blind vias so

that at least some of said first and second signal lines are connected to ~~some~~ said first and second metal layers.

31. (previously presented) The method as claimed in claim 30, wherein the steps of metallizing said through vias and metallizing said blind vias are performed simultaneously.

32. (withdrawn) A method as claimed in claim 29~~28~~, wherein said first metal layer includes a ground plane and said second metal layer includes a power plane.

33. (previously presented) The method as claimed in claim 29, wherein said first signal lines are substantially perpendicular to said second signal lines.

34. (currently amended) The method as claimed in claim 33, wherein ~~the selectively~~ patterning ~~step~~ includes the ~~step of~~ etching said ~~the~~ outer metal layers.

E.1 Concluded